EE143 Lab Week 6 Measurement Checklist:

1) Lithography

Time (sec)	
Softbake:	
Exposure:	
Developer:	
Hardbake:	

Linewidth (um) of Photoresist

Nominal	Measured	% Overetch
2		
3		
4		
8		

Take a photo of the linewidth marks.

Vernier Misalignment:	
X	
Y	

2) Poysilicon:

Polysilicon Sheet Resistance	
Polysilicon Thickness	
Polysilicon Etch Time:	

Linewidth (um) of Polysilicon after etch

Nominal	Measured	% Overetch
2		
3		
4		
8		

3) Measurements after Process Completion:

ACTV Sheet Resistivity (Control Wafer):

Questions:

Calculate % overetch of the linewidth patterns

What were the visual methods for determining completion of etching poly and gate oxide, respectively?

Calculate theoretical substrate doping profile up to this week's thermal step and compare against the substrate sheet resistance measured.